Session 17 Overview

RFID and RF Directions

Chair: Vadim Gutnik, Impinj, Newport Beach, CA

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Radio frequency identification technology is rapidly becoming commercially significant, with volumes in the billions of units per year predicted for the next few years. In this extremely price-sensitive market, chip size is critical, but at the same time, ever more powerful standards and stringent requirements for reliability require MHz data rates. The papers in this session push the frontiers of RFID size and performance. In the second half of the session, mechanical resonators, integrated FBARs and MEMS, promise to integrate high-quality RF filters and oscillators directly with transistors. Novel physical structures enable extremely high-performance oscillators and LNAs.

A 0.15×0.15mm^2 7.5μm-thick RFID chip in a 0.18μm SOI CMOS technology containing a 128b ROM is presented in Paper 17.1. An SOI buried oxide layer structure acts as an etch stop to enable aggressive thinning. Contact to the antenna is made from both top and bottom of the die.

In Paper 17.2, a passive UHF RFID tag, fabricated in 0.35μm FeRAM CMOS technology, with a 36.6% rectifier efficiency is described. This high efficiency is made possible by a CMOS full-wave rectifier with a ferroelectric capacitor. The chip boasts a read and write range of 4.3m and can support read rates of 129 tags/s.

A 3.4Mb/s 13.56MHz RFID front-end is presented in Paper 17.3. The front end uses multi-level signaling and is fabricated in a 6M 0.18μm 1.8V digital CMOS process technology.

The session continues with Paper 17.4, where a novel artificial dielectric is presented which takes the place of an LC tank in a high-quality oscillator. The 60GHz VCO in 90nm CMOS occupies only 0.015mm^2, consumes 1.9mW, and has a measured phase noise of -100dBc/Hz at 1MHz offset.

In Paper 17.5, a 5.4GHz 0.35μm BiCMOS SiGe FBAR oscillator is presented. The resonator is integrated directly above a silicon IC, and achieves a phase noise of -117.7 dBc/Hz at 100kHz offset while drawing 1.7mA from 2.7V.

In Paper 17.6, a single-ended input to balanced output 425MHz electromechanical filter is introduced. The technology provides 1MHz channel-select filtering, while eliminating the need for RF switches and baluns in front-end transceivers, and brings the filter performance to 8dB insertion loss with -50dB stop-band rejection and -48dB common-mode suppression.

A low-power 2.4GHz heterodyne receiver front-end in 0.18μm CMOS using BAW solidly-mounted resonators is presented in Paper 17.7. The resonators, with Qs of up to 580, provide both impedance matching and selectivity. An image rejection of up to 50dB, a noise figure of 11dB and IIP_3 of -16.1dBm with a power dissipation of 1.8mW are demonstrated.

In Paper 17.8, a 0.46mm^2 V-band (50 to 75GHz) CMOS LNA is described. The three-stage cascade CMOS LNA is implemented in 0.13μm CMOS technology, exhibits better than 20dB measured gain from 51 to 57.5 GHz, minimum noise-figure of 7.1dB at 56.8GHz, P_{1dB} of -22dB, and an input IP_3 of -12dBm, under a 2.4V/33mA bias condition.

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17.1 An SOI-Based 7.5μm-Thick 0.15×0.15mm² RFID Chip **1:30 PM**
M. Usami, Hitachi, Tokyo, Japan

A 0.15×0.15mm² RFID chip containing a 128b ROM is fabricated in a 0.18μm 4M SOI CMOS technology. It achieves 480mm read range with a 2.45GHz carrier for a reader output power of 300mW. The chip is thinned precisely by using an SOI buried oxide layer structure as an etch stop. An RFID antenna is connected to the chip by using a double-surface electrode.

17.2 A Passive UHF RFID Tag LSI with 36.6% Efficiency CMOS-Only Rectifier and Current-Mode Demodulator in 0.35μm FeRAM Technology **2:00 PM**
H. Nakamoto, Fujitsu, Kawasaki, Japan

A passive UHF RFID tag LSI in 0.35μm CMOS with 2kb FeRAM enables the 2.9-times higher 32b read-and-write throughput over an EEPROM-based tag. A CMOS full-wave rectifier improves the power efficiency from 16.6% up to 36.6% by lossless internal V_{th} cancellation and mirror stack architecture. A current-mode ASK demodulator converts the 15% power modulation into linear current signal over a 27dB dynamic range of the incoming power.

17.3 A 3.4Mb/s RFID Front-end for Proximity Applications Based on a Delta-modulator **2:30 PM**
B. Gomez, CEA-LETI, Grenoble, France

A 13.56MHz RFID front-end uses multi-level signaling to achieve 3.4Mb/s operation. The circuit is built around a delta-modulator loop which ensures demodulation and ADC functions as well as supply-voltage regulation. The circuits are fabricated in a 6M 0.18μm 1.8V digital CMOS process in an area of <0.5mm².

17.4 A 60GHz CMOS VCO Using On-Chip Resonator with Embedded Artificial Dielectric for Size, Loss, and Noise Reduction **3:15 PM**
D. Huang, University of California, Los Angeles, CA

An on-chip resonator with artificial dielectric in place of the LC tank yields reduced metal/substrate losses, higher resonator Q and a λ/4 length reduction of 4.7 times. The VCO uses 90nm CMOS, with 0.015mm² area, consumes 1.9mW and has a measured phase noise of -100dBc/Hz at 1MHz offset. The FOM is -193dBc/Hz.

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17.5 A 5.4GHz 0.35μm BiCMOS FBAR Resonator Oscillator in Above-IC Technology **3:45 PM**
M. Aissi, LAAS-CNRS, Toulouse, France

A 5.4GHz 0.35μm BiCMOS SiGe FBAR oscillator is presented. The FBAR resonator is directly integrated above the silicon IC, thus eliminating the bond wires and associated parasitics of the classical FBAR oscillators. The oscillator achieves a phase noise of -117.7dBc/Hz at 100kHz offset from 5.46GHz carrier frequency while the oscillator core draws 1.7mA from 2.7V.

17.6 Dielectrically Transduced Single-Ended to Differential MEMS Filter **4:00 PM**
D. Weinstein, Cornell University, Ithaca, NY

A single-ended input to balanced output 425MHz mechanically coupled electromechanical filter is presented. This technology provides 1MHz channel select filtering while eliminating the need for RF switches and baluns in front-end transceivers. The filter achieves 8dB insertion loss with -50dB stop-band rejection and -48dB common-mode suppression.

17.7 A Low-Power 2.4GHz CMOS Receiver Front-End Using BAW Resonators **4:15 PM**
J. Chabloz, CSEM, Neuchâtel, Switzerland

A low-power 2.4GHz heterodyne receiver front-end is integrated in 0.18μm CMOS using BAW solidly mounted resonators. The resonators with Qs of up to 580, provide both impedance matching and selectivity. An image rejection of up to 50dB, a NF of 11dB and IIP3 of -16.1dBm with a power dissipation of 1.8mW are demonstrated.

17.8 A Miniature V-Band 3-Stage Cascode LNA in 0.13μm CMOS **4:45 PM**
H. Wang, National Taiwan University, Taipei, Taiwan

A miniature V-Band (50 to 75GHz) 3-stage cascode CMOS LNA implemented in 0.13μm bulk CMOS technology exhibits better than 20dB measured gain from 51 to 57.5GHz in 0.46mm² die size. The minimum NF is 7.1dB at 56.8GHz. The P_{1dB} is -22dBm, the IIP3 is -12dBm, and the total current is 33mA.